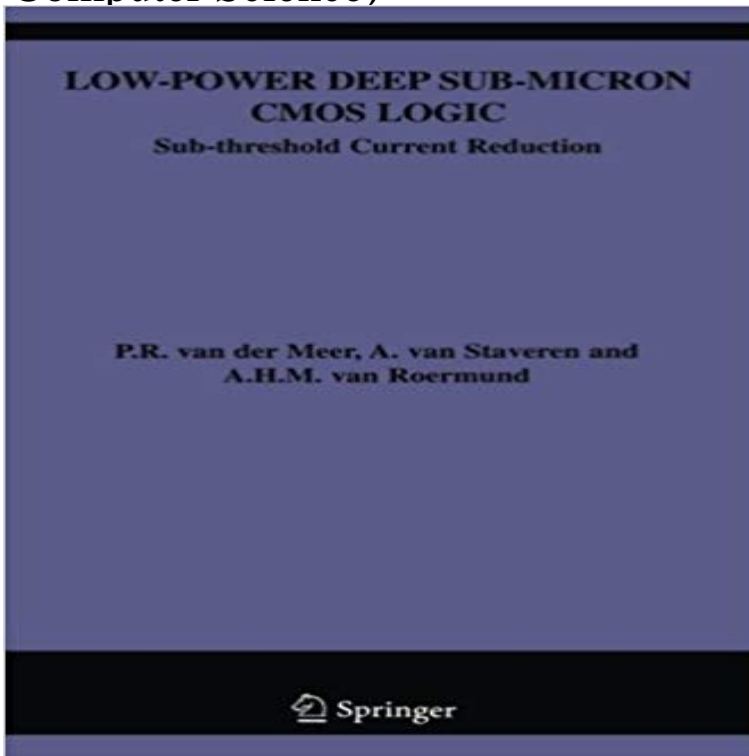


Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction (The Springer International Series in Engineering and Computer Science)



1. 1 Power-dissipation trends in CMOS circuits Shrinking device geometry, growing chip area and increased data-processing speed performance are technological trends in the integrated circuit industry to enlarge chip functionality. Already in 1965 Gordon Moore predicted that the total number of devices on a chip would double every year until the 1970s and every 24 months in the 1980s. This prediction is widely known as Moores Law and eventually culminated in the Semiconductor Industry Association (SIA) technology road map [1]. The SIA road map has been a guide for the industry leading them to continued wafer and die size growth, increased transistor density and operating frequencies, and defect density reduction. To mention a few numbers; the die size increased 7% per year, the smallest feature sizes decreased 30% and the operating frequencies doubled every two years. As a consequence of these trends both the number of transistors and the power dissipation per unit area increase. In the near future the maximum power dissipation per unit area will be reached. Down-scaling of the supply voltage is not only the most effective way to reduce power dissipation in general it also is a necessary precondition to ensure device reliability by reducing electrical fields and device temperature, to prevent device degradation. A draw-back of this solution is an increased signal propagation delay, which results in a lower data-processing speed performance.

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