

Hot Carrier Design Considerations for MOS Devices and Circuits



As device dimensions decrease, hot-carrier effects, which are due mainly to the presence of a high electric field inside the device, are becoming a major design concern. On the one hand, the detrimental effects-such as transconductance degradation and threshold shift-need to be minimized or, if possible, avoided altogether. On the other hand, performance such as the programming efficiency of nonvolatile memories or the carrier velocity inside the devices-need to be maintained or improved through the use of submicron technologies, even in the presence of a reduced power supply. As a result, one of the major challenges facing MOS design engineers today is to harness the hot-carrier effects so that, without sacrificing product performance, degradation can be kept to a minimum and a reliable design obtained. To accomplish this, the physical mechanisms responsible for the degradations should first be experimentally identified and characterized. With adequate models thus obtained, steps can be taken to optimize the design, so that an adequate level of quality assurance in device or circuit performance can be achieved. This book addresses these hot-carrier design issues for MOS devices and circuits, and is used primarily as a professional guide for process development engineers, device engineers, and circuit designers who are interested in the latest developments in hot-carrier degradation modeling and hot-carrier reliability design techniques. It may also be considered as a reference book for graduate students who have some research interests in this exciting, yet sometime controversial, field.

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