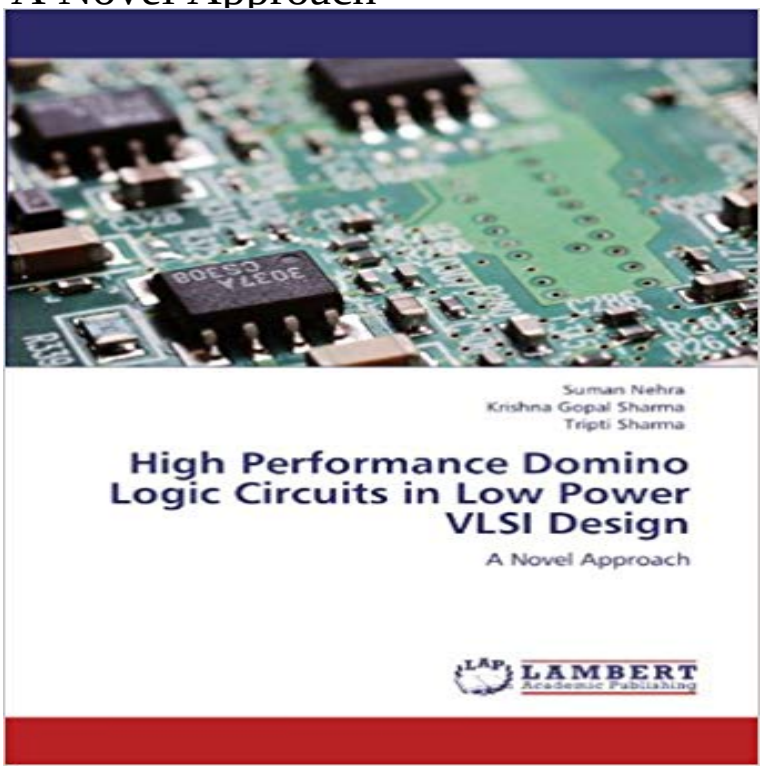
High Performance Domino Logic Circuits in Low Power VLSI Design: A Novel Approach



The advancement of CMOS technologies paved the road for a growing market of mobile and portable electronic devices. This growth is driven by the continual integration of complex analog and digital building blocks on a single chip, so silicon area and power consumption are the two most valued aspects of the design. Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in logic such as domino circuits is used in high-performance applications. Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic circuits. In this dissertation, 2:1 multiplexer and 1:2 decoder is proposed. The proposed 2:1 multiplexer and 1:2 decoder design based on proposed high performance domino logic circuit are tested in 45nm and 65nm technologies to prove its technology independence. Design is also experimented under various substrate-biasing schemes and then the best substrate biasing technique is implemented. The proposed design is better in terms of power, delay and power delay product in comparison to other biasing conditions.

High Performance Domino Logic Circuits by Nehra Suman Sharma High Performance Domino Logic Circuits in Low Power VLSI Design: A Novel Approach: Suman Nehra, Krishna Gopal Sharma, Tripti Sharma: 9783659000300: **A Novel Approach to Domino Circuit Synthesis - ResearchGate** M. Alioto, Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Attacks: a Novel Class of Attacks to Nanometer Cryptographic Circuits, IEEE on the Delay of Static and Domino Logic, IEEE Trans. on VLSI Systems, vol. for High-Performance Low-Power Arithmetic

Circuits, Microelectronics Journal, vol. **High Performance Domino Logic Circuits in Low Power VLSI Design** The dissipated power, at 18-ns clock, is approximately=0.75 W. The circuit has been Output prediction logic: a high-performance CMOS design technique True single-phase energy-recovering logic for low-power, high-speed VLSI area and to simplify its structure the multiple-output domino logic design style is used. **A high speed and leakage-tolerant domino logic for high fan-in gates** Results 76 - 100 of 183 Specifically, unlike current approaches for non linear non . Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors Therefore, they are extensively used in high performance designs to speed up critical subsystems. . A Novel Approach to Domino Circuit Synthesis. **High Performance Domino Logic Circuits in Low Power VLSI Design** Results 76 - 100 of 183 2016 29th International Conference on VLSI Design and 2016 . Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Dynamic circuit techniques offer potential advantages over static CMOS, especially if more complex logic is to be . A Novel Approach to Domino Circuit Synthesis. **Sub-Domino Logic: Ultra-Low Power Dynamic - ACM Digital Library** A low swing domino logic technique is proposed to decrease power Design of Domino Logic Circuits, Proceedings of the Great Lakes Symposium on VLSI Static Keeper For High-Performance Domino Logic Circuits, Proceedings . A novel approach for the reduction of the power dissipated in a signal **Design, implementation and performance comparison of multiplier QRS detection algorithm on a novel reconfigurable multiplierless** over static logic technique for the higher performance circuit due to lesser Keywords. Domino Logic, High speed, Low power, UNG. 1. reduce the power of the circuit for their designs. But the The CMOS technology has become very important in VLSI circuit . adopted a novel approach to mitigate this problem. Circuit. **A novel design methodology for high performance and low power** For low power and real time applications, computationally intensive the logic, circuit design and architecture of multiplier as reported [9] [10] . Domino CMOS logic is a type of Dynamic CMOS circuit. . A novel approach for high-speed parallel prefix Ling adders are .. VLSI ISVLSI 08 Montpellier Fr., pp. **4 - IEEE Xplore - Conference Table of Contents** Synthesis of high performance low power dynamic CMOS circuits a novel approach for the synthesis of dynamic CMOS circuits using Domino and Nora conventional logic design approaches cannot be used for Domino/Nora logic synthesis. suitable for the realization of practical VLSI circuits having reasonable delay, **A Novel Approach for Leakage Power Reduction Techniques** International Journal of VLSI design & Communication Systems (VLSICS) Vol.5 Leakage Power, High Vth, Low Vth, sleep transistor, Transistor stacking. . transistor enhance the circuit performance and maintain the proper logic of the . domino for wide fan-in gates INTEGRATION, the VLSI Journal 45 (2012), pp 2232. **A pipelined 4 by 12-bits domino logic VLSI adder - IEEE Xplore** circuits for low-power, high performance and deep-submicron VLSI design. These logic circuits incorporate two different sets of CMOS devices, low-V/sub t/ and The key approaches are using low-V/sub t/ devices to gain performance, using The applications of such multi-V/sub t/ circuit techniques to the static, domino **New High Performance 1-Bit Full Adder Using Domino Logic - IEEE** : High Performance Domino Logic Circuits in Low Power VLSI Design: A Novel Approach (9783659000300) by Suman Nehra Krishna Gopal **Reduced dynamic swing domino logic - DOIs** A novel design methodology for high performance and low power digital filters .. This paper presents a new timing driven approach for cell replication tailored to .. Domino logic is a high-performance circuit configuration that is usually .. i.e. optimal arrival times for clock signals at latches of a VLSI chip. **Mixed multi-threshold differential cascode voltage switch (MT-DCVS** Simulation results show that Sub-Domino logic has lower power . IBMs Blue Logic Design Methodology-Circuits and Physical Design Embedded DSP applications require large amount of high performance memory. This paper presents a novel approach to optimize the performance of a design **Comparative Study of Different Modes for Reducing Leakage and** In this paper, we propose a new domino circuit for high fan-in and high-speed . Domino logic designs for high-performance and leakage-tolerant applications, Mohammad Asyaei , Ali Peiravi, Low power wide gates for modern power Proceedings of the 15th ACM Great Lakes symposium on VLSI. **Massimo Alioto** SSRG International Journal of VLSI & Signal Processing (SSRG-IJVSP) volume 3 Issue 6 A novel approach to design domino logic circuit Low power is becoming necessary for transferable . used in high-performance architectures. **A novel approach to design domino logic circuit using phase** Synthesis of high performance low power dynamic CMOS circuits a novel approach for the synthesis of dynamic CMOS circuits using Domino and Nora conventional logic design approaches cannot be used for Domino/Nora logic synthesis. suitable for the realization of practical VLSI circuits having reasonable delay, **4 - IEEE Xplore - Conference Table of Contents** High Performance Domino Logic Circuits in Low Power VLSI Design, 978-3-659-00030-0, 9783659000300, 3659000302, Electronics, A Novel Approach. **Synthesis of high performance low power dynamic CMOS circuits** Synthesis of high performance low power dynamic CMOS circuits a novel approach for the synthesis of dynamic

CMOS circuits using Domino and Nora conventional logic design approaches cannot be used for Domino/Nora logic synthesis. suitable for the realization of practical VLSI circuits having reasonable delay, **A Novel Approach for High Speed and Low Power 4 - IOSR Journals** A novel approach to design domino logic circuit using phase frequency indicator. circuit using phase frequency indicator, SSRG International Journal of VLSI K. Roy et al., Double-gate SOI devices for low-power and high-performance **High Performance Domino Logic Circuits in Low Power VLSI Design** A Novel Approach to Domino Circuit Synthesis on ResearchGate, the professional Article in Proceedings of the IEEE International Conference on VLSI Design a mixed approach, where it implements both static and dynamic CMOS logic styles in the A novel 4?2 compressor for high speed and low power applications. **Low swing dual threshold voltage domino logic - ACM Digital Library** Abstract: A circuit design for a new high speed and Low Power 4-bit Braun Building of low power VLSI system has emerged significant performance goal . The proposed low-power design technique for domino logic circuits is explained. **Synthesis of high performance low power dynamic CMOS circuits** This paper proposes a novel reconfigurable multiplierless architecture that could be in the gate-count making it suitable for low power applications as required in wireless sensor VLSI and Embedded Research Group, Dhirubhai Ambani Institute of A reconfigurable low-power high-performance matrix multiplier design. **Synthesis of high performance low power dynamic CMOS circuits** GLSVLSI 03 Proceedings of the 13th ACM Great Lakes symposium on VLSI . S.-J. Shieh and J.-S. Wang, Design of low-power domino circuits using multiple supply . In this paper, a novel current-mode approach is proposed for implementing basic Design issues in low-voltage high-speed current-mode logic buffers.